23

$ AF 330.00

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
MCT.0078US

In Re Application Of: **Paul A. LaBerge**

Serial No.	Filing Date	Examiner	Group Art Unit
09/363,605	07/29/99	Xuong M. Chung-Trans	2833

Invention: **Capturing Read Data**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **November 14, 2003.**

The fee for filing this Appeal Brief is: **$330.00**

☒ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**

Signature

Dated: **November 17, 2003**

Fred. G. Pruner, Jr., Reg. No. 40,779
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, Texas 77024
(713) 468-8880
(713) 468-8883 (fax)

I certify that this document and fee is being deposited on **November 17, 2003** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature of Person Mailing Correspondence

Janice Munoz

Typed or Printed Name of Person Mailing Correspondence

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Paul A. LaBerge	§	Art Unit:	2833
Serial No.:	09/363,605	§	Examiner:	Xuong M. Chung-Trans
Filed:	July 29, 1999	§		
Title:	Capturing Read Data	§	Docket No.	MCT.0078US (70-0130.00/US)

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated October 9, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

Date of Deposit November 17, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Janice Munoz

III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-26. During prosecution, claims 24 and 25 were cancelled; and claims 27 and 28 were added. Claims 6, 14, 27 and 28 are objected as being dependent upon rejected base claims but are indicated as being allowable if rewritten in independent form. Claims 1-5, 8-13 and 15-26 have been finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

There are no unentered amendments.

V. SUMMARY OF THE INVENTION

Referring to Fig. 6, an embodiment 30 of a computer system in accordance with the invention includes a north bridge 34 that is adapted to minimize read latency that is introduced by the north bridge 34. In particular, a local bus interface 60 of the bridge 34 includes a buffer 42 that is adapted to capture read data directly from a memory bus 41. Thus, the read data is captured near a local bus 33 (and not near the memory bus 41), an arrangement that may reduce the number of internal clock cycles (of the bridge 34) that elapse in the transfer of data from the memory bus 41 to the buffer 42. Specification, p. 4.

For example, a processor 32 (a central processing unit (CPU), as an example) may furnish signals to the local bus 33 to indicate a memory read operation. In response to the signals on the local bus 33, the bridge 34 may generate signals on the memory bus 41 to initiate a read operation with a system memory 44. In this manner, in the course of the

memory read operation, the system memory 44 furnishes signals (to the memory bus 41) that indicate the requested read data. Unlike conventional bridges, the bridge 34 bypasses a memory bus interface 64 (of the bridge 34) and captures the read data directly into the buffer 42 of the local bus interface 60. Specification, p. 4.

Referring to Fig. 7, more particularly, unlike conventional arrangements, the bridge 34 effectively extends the memory channel provided by the memory bus 41 inside the bridge 34. In this manner, the data and strobe lines of the memory bus 41 (via internal data and data strobe conductive traces, or lines 80) are effectively extended by placing the buffer 42 closer to the local bus 33 than to the memory bus 41. As a result of this arrangement, a much smaller asynchronous propagation delay is incurred in the transfer of data from the buffer 42 to the local bus 33, as compared to the asynchronous delay encountered in a conventional bridge in which the data is transferred from a memory bus interface (where the data is captured) to a local bus interface. Specification, pp. 4-5.

Thus, the transfer of read data through a conventional bridge circuit includes two latching events to compensate for asynchronous propagation delays: one latching event to capture the read data into a memory bus interface (that is located near the memory bus) and another latching event to capture the data in a local bus interface (that is located near the local bus) after the data propagates between the memory and local bus interfaces. Each of these latching events, in turn, consumes internal clock cycles of the conventional bridge, as each latching event must accommodate the worst case delay scenario. However, unlike this conventional arrangement, the bridge 34 compensates for the

asynchronous delays that are introduced by the memory bus 41 and the data and data strobe lines 80 in one latching event. Thus, the bridge 34 provides a more efficient arrangement that may permit the data to be communicated across the bridge 34 in a fewer number of internal clock cycles, as compared to conventional bridges. Specification, p. 5.

In some embodiments, the memory 44 may be formed from double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices (double inline memory modules (DIMMs), for example), and the memory bus 41 may be a DDR memory bus. For these embodiments, the DQS data strobe signals from the memory bus 41 may be used to synchronize the capture of the data from the bus 41, as described below. For these embodiments, the local bus interface 60 may include a delay circuit 61 to align the edges of the DQS signals with the "data eyes" of the signals that indicate the data for purposes of capturing valid data from the memory bus 41. The delay circuit 61 may be initially programmed by execution of a basic input/output system (BIOS) during bootup of the computer system 30, and thereafter, the delay circuit 61 may regulate the introduced delay(s) to compensate for changing voltages and temperatures, factors that may affect the delay(s). Specification, p. 5.

Among the other features of the bridge 34, the memory bus interface 64 may include a write buffer 72 for furnishing memory write data to the memory bus 41. The memory bus interface 64 may also include a memory controller 70 that furnishes signals (clock signals and control signals, as examples) to the memory bus 41 to perform selected memory bus operations (read, write and refresh operations, as examples) with the system

memory 44. The local bus interface 60 may include a local bus controller 65 that, among other things, furnishes signals to encode and decode bus cycles on the local bus 33. A driver 83 of the bridge 34 may be coupled to the data and data strobe lines of the memory bus 41 and furnish signals that indicate the voltages of these lines to the end of the lines 80 closest to the memory bus 41. Specification, pp. 5-6.

Other bus interfaces of the bridge 34 may include an Accelerated Graphics Port (AGP) bus interface 68 and a Peripheral Component Interconnect (PCI) bus interface 66. The AGP is described in detail in the Accelerated Graphics Port Interface Specification, Revision 1.0, published on July 31, 1996, by Intel Corporation of Santa Clara, California. The PCI Specification is available from the PCI Special Interest Group, Portland, Oregon 97214. Specification, p. 6.

Referring to Fig. 8, in some embodiments, the memory bus 41 may include sixty-four data lines that may be used to communicate sixty-four bits of data (i.e., one double Dword, or Qword) that are represented by the notation D[63:0], and the buffer 42 may include a bit buffer 100 for each data line of the memory bus 41. In some embodiments, each bit buffer 100 may store up to eight bits of data from eight respective Qwords that appear on the memory bus 41. Thus, collectively, in some embodiments, the sixty-four bit buffers 100 may store up to two cache lines (i.e., 64 bytes) of data. Two Qwords may be simultaneously retrieved from the bit buffers 100: an upper address Qword that is furnished by upper bit lines 110 (one upper bit line 110 per bit buffer 100) and a lower address Qword that is furnished by lower bits lines 112 (one lower bit line 112 per bit buffer 100). Specification, p. 6.

Each bit buffer 100 latches its respective data bits on the positive and negative edges of a DQS data strobe signal. Different bit buffers 100 may receive different DQS signals from the lines 80. In this manner, the lines 80 are arranged so that each DQS signal experiences approximately the same delay as an associated group of the data signals. Thus, a particular DQS signal may be used to latch the bit buffers 100 that receive the data signals that are associated with the DQS signal. Specification, p. 6.

The bit buffers 100 begin furnishing the latched bits to the bit lines 110 and 112 in synchronization with an internal clock signal (called CLK) when a read enable signal (called RD_EN) is asserted. Because the bit buffers 100 may store several entries (eight, for example) and the CLK signal may have a higher frequency (double the frequency, for example) than the frequency of the DQS strobe (when active), a sufficient number of cycles of the CLK signal may be permitted to elapse before the latched data is retrieved from the buffers 100 in order to ensure that the latched data is valid. Specification, p. 6.

The upper 110 and lower 112 bit lines may be coupled to input terminals of a multi-bit multiplexer 102. Other input terminals 101 of the multiplexer 102 may be coupled to the multiplexing circuitry 62 for purposes of receiving data captured by the AGP 68 or PCI 66 bus interfaces. The selection of the data from either the bit buffers 100, the AGP interface 68, or the PCI bus interface 66 may be controlled by, for example, selection lines 103 that are coupled to the multiplexing circuitry 62. In some embodiments, the output terminals of the multiplexer 102 are coupled to a buffer 104 that stores data to be furnished to the local bus 33. Specification, p. 7.

The local bus interface 60 may also include the local bus controller 65, an input/output (I/O) interface 105 for driving and buffering signals to/from the local bus 33 and write path circuitry 108. Specification, p. 7.

Referring to Fig. 9, as an example, in some embodiments, the bit buffer 100a that receives the D[0] bit may have the following design that is similar to the design of the other bit buffers 100. In particular, in some embodiments, the bit buffer 100a may include lower Qword bit latches 120 that store the lowest order bits D[0] for the lower Qwords and upper Qword bit latches 124 that store the lowest order bits D[0] for the upper Qwords. The lower Qword bit latches 120 capture the D[0] bit on positive edges of the DQS signal when their respective latch enable signal (L[0], L[2], L[4] or L[6]) is asserted, and the upper Qword bit latches 124 capture the D[0] bit on negative edges of the DQS signal when their respective latch enable signal (L[1], L[3], L[5] or L[7]) is asserted. Each latch enable signal is asserted for a different edge of the DQS signal, and thus the different latches 120, 124 store bits for Qwords from eight different memory locations. Specification, p. 7.

The bit latch 100a may include a multi-bit multiplexer 126 that is coupled to the output terminals of the upper Qword bit latches 120 and a multi-bit multiplexer 128 that is coupled to the output terminals of the lower Qword bit latches 124. The multiplexer 126 provides the upper bit line 110 of the bit latch 100a, and the multiplexer 128 provides the lower bit line 112 of the bit latch 100a. The select terminals of both multiplexers 126 and 128 receive the same signals from a counter 130 that is clocked by the CLK signal. When the counter 130 is enabled (by the assertion of the RD_EN read enable signal), the

counter 130 controls the multiplexers 126 and 128 so that the D[0] bits for the upper and lower Qword pair are provided at the same time. The bit latch 100a may include latch enable logic 132 that furnishes the latch enable signals. The latch enable logic 132 is clocked by the DQS signal. Specification, p. 7.

Referring back to Fig. 6, beside the components described above, the computer system 30 may also include a display controller 45 that is coupled to the AGP bus 43 and controls a display 47. A modem 46, for example, may be coupled to the PCI bus 38 along with a south bridge 36. The south bridge 36 may provide an interface to an I/O expansion bus 40, a hard disk drive 48 and a CD-ROM 50. An I/O controller 54 may be coupled to the I/O expansion bus 40 and receive input from a mouse 56 and a keyboard 58. The I/O controller 54 may further control the operation of a floppy disk drive 52. Specification, p. 8.

In this context of this application, the term "processor" may generally refer to at least one central processing unit (CPU), microcontroller or microprocessor, as just a few examples. The phrase "computer system" may refer to any type of processor-based system, such as a desktop computer or a laptop computer, as just a few examples. Thus, the invention is not intended to be limited to the illustrated computer system 30, but rather, the computer system is an example of one of many possible embodiments. Specification, p. 8.

VI. ISSUES

A. Can claims 1-5 and 7-10 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

B. Can claims 11-13 and 15-17 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 11?

C. Can claims 18-21 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 18?

D. Can claims 22, 23 and 26 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 22?

VII. GROUPING OF THE CLAIMS

Claims 1-5 and 7-10 can be grouped together; claims 11-13 and 15-17 can be grouped together; claims 18-21 can be grouped together; and claims 22, 23 and 26 can be grouped together. With this grouping, all claims of a particular group stand or fall together. Furthermore, regardless of the grouping that is set forth by the Examiner's rejections, the claims of each group set forth in this section stand alone with respect to the claims of the other groups that are set forth in this section. In other words, any claim of a particular group that is set forth in this section does not stand or fall together with any claim of any other group that is set forth in this section.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Can claims 1-5 and 7-10 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

The computer system of claim 1 includes a local bus, a memory bus and a buffer. The memory bus is capable of indicating data; and the buffer is adapted to capture the data directly from the memory bus. The buffer is located closer to the local bus than to the memory bus.

The Examiner rejects independent claim 1 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,623,635 (hereinafter called "Chen") in view of U.S. Patent No. 6,505,305 (hereinafter called "Olarig"). Chen is generally directed to a bridge that transfers data from an input/output (I/O) device to a main memory. Olarig generally discloses a computer system that has a fail-over feature to handle memory access errors.

In the § 103 rejection of claim 1, the Examiner relies on Chen to allegedly a local bus, a memory bus and a buffer. Referring to Figure 1 of Chen, the Examiner labels the CPU 12 as the alleged local bus, the memory bus 18 as the alleged memory bus of claim 1 and a buffer 21 in an I/O bridge 22 as the alleged buffer of claim 1. Office Action Mailed on April 8, 2003 (hereinafter referred to as "the Second Office Action"), p. 2. The Examiner states, "Chen does not explicitly disclose that the buffer being located closer to the local bus than to the memory bus." Second Office Action, pp. 2-3. However, the Examiner concludes that it would have been obvious for one skilled in the

art to modify Chen in view of Olarig so that the buffer 21 of the I/O bridge 22 is closer to a local bus than to the memory bus 18.

Referring to Olarig, Olarig discloses a computer system in Figure 3 that includes a first bus 204 and a second bus 208. A bridge 206 is located between the first 204 and second 208 buses. Another bridge 202 connects the first bus 204 to a processor bus P_B. A processor 200 is connected to this processor bus P_B. In the description of Figure 3, Olarig states, "since the first bus 204 is physically closer to the processor 200 than is the second bus 208, it is typically able to transfer information to/from the processor 200 or the memory system 230 more quickly than can the second bus 208." Olarig, 6:32-36. The Examiner contends that this cited passage from Olarig supplies the alleged suggestion or motivation to modify Chen so that Chen's I/O bridge buffer 21 is moved closer to a local bus than to the memory bus 18. Office Action Mailed on October 9, 2003 (hereinafter called "the Final Office Action"), pp. 2-3.

A *prima facie* case of obviousness based on the modification of a reference requires the Examiner to show where the prior art contains the alleged suggestion or motivation for the modification, as "obviousness cannot be predicated on what is unknown." *In re Spormann*, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966); M.P.E.P. § 2143.. The Examiner, having knowledge of the invention, contends that the proposed modification to Chen would have been obvious to one of skill in the art. This conclusion, however, must be supported by specific references to the prior art, as a *prima facie* case of obviousness requires the Examiner to show that one skilled in the art, without knowledge of the claimed invention, would have been motivated to modify Chen

to derive the claimed invention. The Examiner has failed to satisfy this requirement, for the reasons set forth below.

As noted above, the Examiner relies on Chen to allegedly teach the local bus of claim 1. However, the CPU 12 of Chen (the alleged local bus) is not a local bus. Thus, for at least the reason that the Examiner fails to show the existence of a suggestion or motivation in the art to modify Chen so that Chen's computer system has a local bus, a *prima facie* case of obviousness has not been established for independent claim 1.

The Examiner fails to establish a *prima facie* case of obviousness for claim 1 for at least the additional, independent reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation to modify Chen so that Chen's I/O bridge buffer 21 is located closer to the memory bus 18 than to a local bus. Contrary to the Examiner's conclusion, Olarig merely stands for the proposition that to access the processor or memory of a computer system, a device that is connected to a bus that is closer to the processor or memory may access the processor or memory faster than a device that is connected to another bus that is located farther away from the processor or memory. This stands to reason, as the farther a bus is from the processor or memory, the greater the number of bridges that are located between the bus and the processor or memory.

Olarig does not, however, provide the requisite suggestion or motivation to modify Chen's I/O bridge buffer 21 to be closer to a local bus than to the memory bus 18 for at least the reason that Olarig merely teaches closer buses provide faster accesses to the processor or memory. The claimed invention is not, however, directed to the

placement of buses. Rather, the claimed invention is directed to the location of a buffer that captures data directly from a memory bus.

Even assuming, *arguendo*, that Olarig stands for the proposition that to decrease access time a device must be positioned closer to the bus being accessed than to another bus, this teaching would also not supply the alleged suggestion or motivation to modify Chen to derive the claimed invention. More specifically, referring to Chen, this reasoning would have led one of skill in the art to place the buffer 21 closer to the *memory bus* 18, contrary to the explicit limitations of claim 1, because the buffer 21 communicates with the *memory bus* 18 (emphasis added). Furthermore, there is no reason or suggestion from Olarig to place Chen's I/O bridge buffer 21 closer to a *local bus*, as the buffer 21 is not even connected to a local bus, which, as set forth above, is not even disclosed in Chen.

Thus, the Examiner fails to show where the prior art contains the alleged suggestion or motivation to modify Chen to derive the claimed invention. As such, the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1. Claims 2-5 and 7-10 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103 rejections of claims 1-5 and 7-10 are improper and should be reversed.

B. Can claims 11-13 and 15-17 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 11?

The bridge of claim 11 is for use with a local bus and a memory bus that is capable of indicating data. The bridge includes conductive traces that are adapted to communicate indications of the data from a first region closer to the memory bus than the local bus to a second region that is located closer to the local bus than to the memory bus. The bridge includes a local bus interface as located closer to the local bus than to the memory bus. The local bus interface includes a buffer that is adapted to capture the indications of the data from the conductive traces near the second region to directly capture the data from the memory bus.

The Examiner rejects independent claim 11 under 35 U.S.C. § 103(a) in view of Chen and Olarig. More specifically, the Examiner relies on Chen to allegedly teach all limitations except for the local bus interface being located closer to the local bus than to the memory bus, where the local bus interface includes a buffer that is adapted to capture indications of the data from a region that is located closer to the local bus than to the memory bus.

Thus, the § 103 rejection of independent claim 11 requires the modification of Chen so that 1. Chen's computer system includes a local bus; and 2. Chen's I/O bridge buffer 21 is moved closer to this local bus than to the memory bus 18.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 11 for at least the reason that the Examiner fails to show where the prior art

contains the alleged suggestion or motivation to modify Chen so that Chen's computer system has a local bus.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 11 for at least the additional, independent reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation to modify Chen so that Chen's I/O bridge buffer 18 is located closer to a local bus than to the memory bus 18. The language cited from Olarig stands for the proposition that a device that is connected to a bus that is located closer to a processor or memory promotes faster access to the processor or memory than a bus that is located farther away from the processor or memory. However, neither this cited language from Olarig nor any other part of Olarig fails to provide a suggestion or motivation to modify Chen to derive the claimed invention. More specifically, Olarig addresses the location of buses, not the location of a buffer relative to buses.

Furthermore, even if, *arguendo*, Olarig stands for placing a device closer to a memory or processor if the device accesses the memory or processor, this teaching does not supply the a suggestion or motivation for modifying Chen so that Chen's I/O bridge buffer 18 is moved closer to a local bus than the memory bus 18. More specifically, the I/O bridge buffer 21 of Olarig captures data from the memory bus 18. Thus, at best, in view of the teaching of Olarig, one skilled in the art would have been motivated to locate the buffer 21 closer to the memory bus 18 instead of a local bus, contrary to the limitations of claim 11. Thus, the Examiner has failed to show where the prior art

contains the alleged suggestion or motivation to modify Chen so that the buffer 21 is located closer to the memory bus 18 than to a local bus.

Claims 12, 13 and 15-17 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103 rejections of claims 11-13 and 15-17 are improper and should be reversed.

C. Can claims 18-21 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 18?

The method of claim 18 is usable with a computer system that includes a local bus and a memory bus. The method includes furnishing data to the memory bus in a memory read operation and capturing the data directly from the memory bus in a buffer that is located closer to the local bus than to the memory bus.

The Examiner rejects independent claim 18 under 35 U.S.C. § 103 in view of the combination of Chen and Olarig. However, the Examiner fails to establish a prima facie case of obvious for independent claim 18 for at least two reasons: 1. there is no suggestion or motivation to modify Chen so that Chen's system has a local bus; and 2. there is no suggestion or motivation to modify Chen's system so that the I/O bridge buffer 21 that is connected to the memory bus 18 is located closer to a local bus than to the memory bus 18. As set forth above, modifying Chen in view of Olarig would render the opposite result: moving the buffer 21 closer to the memory bus 18 than to a local bus.

Claims 19-21 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103 rejections of claims 18-21 are improper and should be reversed.

D. Can claims 22, 23 and 26 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 22?

The method of claim 22 is usable with a computer system and includes extending a memory bus into a bridge. The memory bus is adapted to indicate data in a memory read operation. The method includes capturing the data directly from the extension of the memory bus into the bridge.

The Examiner rejects independent claim 22 under 35 U.S.C. § 103(a) in view of the combination of Chen and Olarig. However, neither one of these references teaches or suggests extending a memory bus into a bridge. More specifically, both Chen and Olarig disclose bridges. Chen discloses a bridge and a memory bus. However, neither one of these references teaches or suggests extending a memory bus into a bridge. The Examiner does not even address where Chen or Olarig allegedly teach these limitations in either of the office actions in which Chen and/or Olarig were applied against independent claim 22. "Obviousness cannot be predicated on what is unknown." *In re Spormann*, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966). Thus, for at least the reason that the Examiner fails to show where the prior art teaches or suggests all claim limitations, a *prima facie* case of obviousness has not been set forth for independent claim 22.

Claims 23 and 26 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, the § 103 rejections of claims 22, 23 and 26 are improper and should be reversed.

IX. CONCLUSION

Applicant requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: November 17, 2003

Fred G. Pruner, Jr., Reg. No. 40,779
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, TX 77024-1805
713/468-8880 [Phone]
713/468-8883 [Facsimile]

APPENDIX OF CLAIMS

The claims on appeal are:

1. A computer system comprising:

a local bus;

a memory bus capable of indicating data; and

a buffer adapted to capture the data directly from the memory bus, the buffer being located closer to the local bus than to the memory bus.

2. The computer system of claim 1, wherein

the memory bus is capable of indicating a data strobe signal, and

the buffer is adapted to latch the data from the memory bus in response to the data strobe signal.

3. The computer system of claim 1, further comprising:

conductive traces adapted to communicate indications of the data from a first region located closer to the memory bus than to the buffer to a second region located closer to the buffer than to the memory bus, the conductive traces introducing an approximate first asynchronous propagation delay in the communication.

4. The computer system of claim 3, further comprising:

circuitry adapted to transfer the data from the buffer to the local bus without introducing a second propagation asynchronous propagation delay that is greater than the first asynchronous propagation delay.

5. The computer system of claim 1, wherein the buffer is part of a local bus interface.

6. The computer system of claim 1, further comprising:

circuitry adapted to transfer the data from the buffer to the local bus, at least a portion of the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

7. The computer system of claim 1, wherein the buffer is part of a local bus interface that is coupled to the local bus, the computer system further comprising:

a third bus;

a fourth bus;

a third bus interface coupled to communicate with the third bus;

a fourth bus interface coupled to communicate with the fourth bus; and

a multiplexing circuit adapted to selectively cause the buffer to store other data from the third and fourth bus interfaces.

8. The computer system of claim 1, wherein the buffer is part of a local bus interface that is located closer to the local bus than to the memory bus.

9. The computer system of claim 8, wherein the local bus interface further comprises:

a local bus controller adapted to use the buffer to furnish signals to the local bus that indicate the data.

10. The computer system of claim 1, further comprising:

a memory interface located closer to the memory bus than to the local bus, the memory interface including another buffer to store other data to be furnished to the memory bus.

11. A bridge for use with a local bus and a memory bus capable of indicating data, comprising:

conductive traces adapted to communicate indications of the data from a first region closer to the memory bus than the local bus to a second region located closer to the local bus than to the memory bus; and

a local bus interface being located closer to the local bus than to the memory bus, the local bus interface including a buffer adapted to capture the indications of the data from the conductive traces near the second region to directly capture the data from the memory bus.

12. The bridge of claim 11, wherein

the memory bus is capable of indicating a data strobe signal, and

the buffer is adapted to latch the data in response to the data strobe signal.

13. The bridge of claim 11, wherein the conductive traces introduce a first asynchronous propagation delay to the indications of the data, the bridge further comprising:

circuitry adapted to transfer the data from the buffer to the local bus without introducing a second asynchronous propagation delay that is greater than the first asynchronous propagation delay.

14. The bridge of claim 13, further comprising:

circuitry adapted to transfer the data from the buffer to the local bus, at least a portion of the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

15. The bridge of claim 12, further comprising:

a third bus;

a fourth bus;

a third bus interface coupled to communicate with the third bus;

a fourth bus interface coupled to communicate with the fourth bus; and

a multiplexing circuit adapted to selectively cause the buffer to store other data from the third and fourth bus interfaces.

16. The bridge of claim 12, wherein the local bus interface further comprises:

a local bus controller adapted to use the buffer to furnish signals to the local bus that indicate the data.

17. The bridge of claim 12, further comprising:

a memory interface located spatially closer to the memory bus than to the local bus, the memory interface including another buffer to store other data to be furnished to the memory bus.

18. A method usable with a computer system that includes a local bus and a memory bus, the method comprising:

furnishing data to the memory bus in a memory read operation; and

capturing the data directly from the memory bus in a buffer that is located closer to the local bus than to the memory bus.

19. The method of claim 18, wherein the act of capturing comprises:

latching the data from the memory bus in response to a data strobe signal of the memory bus.

20. The method of claim 18, further comprising:

using conductive traces adapted to communicate indications of the data from a first region located closer to the memory bus than to the buffer to a second region located closer to the buffer than to the memory bus, the conductive lines introducing an approximate first asynchronous propagation delay in the communication.

21. The method of claim 20, further comprising:

transferring the data from the buffer to the local bus without introducing a second asynchronous propagation delay that is greater than the first asynchronous propagation delay.

22. A method usable with a computer system, comprising:

extending a memory bus into a bridge, the memory bus being adapted to indicate data in a memory read operation; and

capturing the data directly from the extension of the memory bus into the bridge.

23. The method of claim 22, wherein the act of capturing comprises:

latching the data from the extension of the memory bus in response to a data strobe signal of the memory bus.

26. The method of claim 22, wherein the act of extending comprises:

extending the memory bus into the bridge so that the extended end of the memory bus is closer to a local bus than to the portion of the memory bus that is located outside of the bridge.

27. The method of claim 18, further comprising:

transferring the data from the buffer to the local bus; and

synchronizing the transferring to a clock signal,

wherein the transferring occurs without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

28. The method of claim 22, further comprising:

transferring the data from a buffer to a local bus, the buffer being located closer to the memory bus than to the local bus; and

synchronizing the transferring to a clock signal,

wherein the transferring occurs without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.